Low Dark Current UV-VIS Planar- electrode Perovskite CMOS Image Sensor

Yan-Rung Lin[1], Pei-Wen Yen[1], Sheng-Min Yu[2], Shiu-Cheng Lou[1], Kai-Ping Chuang[1], Bor-Nian Chuang[1]
Industrial Technology Research Institute
Center for Measurement Standards[1], Material and Chemical Research Laboratories[2], Hsinchu, Taiwan
Yen-Chih Chiou[3], Chih-Cheng Hsieh[3], Cheng-Hung Hou[4], Feng-Yu Tsai[4]
National Tsing Hua University, Department of Electrical Engineering[3], Hsinchu, Taiwan
National Taiwan University, Department of Materials Science and Engineering[4], Taipei, Taiwan

We proposed a planar-electrode structure hybrid CIS (CMOS image sensor) with a thin organic-inorganic perovskite layer as a photoactive material. A quiet low dark current ranging from 2 pA/cm^2 at 0.2 V and 10 nA/cm^2 at 2V was achieved by the aid of titanium dioxide (TiO_2) layer between the electrode aluminum (Al) and perovskite (PVSK) film. In order to evaluate the process integration and device characterization, the dummy chip of planar–electrode type pixel photodetectors was fabricated by lithography. More than 1000% external quantum efficiency (EQE) was observed in the planar-electrode photodetector structure in which Al electrodes capped with titanium nitride (TiN). The PVSK photodetectors have a high photoconductive gain, broad spectral response, low temperature process and simple structure. It demonstrated a possibility of using the hybrid active layer perovskite for UV enhanced and next generation sensor.

MOTIVATION

In the requirement of more pixels and smaller modules in image sensors for consumer products, the technology of the image sensor structure transferred from FSI (Front side illumination) to BSI (Back side illumination) for smaller pixel (< 1.4um) and high performance. How to obtain higher quantum efficiency (QE) and to increase the optical efficiency on the sensor are critical issues in the development of image sensor for smaller pixels. Some researchers were devoted to replace the photoactive silicon by organic or hybrid materials[1-3] which can be vertically deposited a thin film on the top of the electronics circuits. This thin film method is effectively to enhance optical efficiency in the pixel by improving the fill factor and photo-electric conversion efficiency while offering a simply and cheap fabrication process.

PVSK has gained rich attention due to its excellent intrinsic properties, including a large absorption coefficient and long carrier diffusion length. That makes it as a candidate for the thin film photoactive layer of CIS. Comparing to vertical structure, the planar structure has a simpler configuration and no loss of the incident light in the top electrode. It shows that they can be low-cost, large area, thin, lightweight photodetectors. So they have opportunity to be implanted in the IoT application. PVSK photodetectors exhibited some unique features such high external quantum efficiency (EQE) in the spectral range from 300 to 800 nm. The absorption coefficient is high in the order of 10^4 cm^{-1}, so a large amount of light can be absorbed with only hundreds of nanometers thickness, which makes optical crosstalk effect unobvious in the photoactive layer. However, most of this type of high gain photodetector suffers from the large dark current and noise, which will limit the application. Some methods were proposed to suppress the dark current [4-5] : to reduce the trap density or to have a good quality film in the photoactive layer or in the interface. In this paper we deposited a blocking layer between the electrode and the photoactive layer to reduce the injection current from the electrode in a biased operation.

EXPERIMENTS AND RESULTS

Device Fabrication

In order to detail evaluate the pixel device characteristic, the dummy chip was designed and fabricated on silicon wafer. Figure 1 is the dummy device structure. Planar aluminum electrodes in the comb shape capped with TiN were first patterned by the lithography process on a silicon wafer covered with a 500 nm thick SiO_2. The electrode line width and gap was 400 nm and 2 μm, respectively. And the pixel area was 25x25 μm^2. It was a 2x27 array. A 350-400 nm photoactive layer, perovskite film $CH_3NH_3PbI_3$, was deposited on it. Then, the chip was encapsulated with a spin-coated film of CYTOP (Asahi Glass).

This perovskite CMOS chip was the test bench for the realization of the CIS design concept and fabrication process. Figure 2 shows the photo of the CMOS PVSK chip and the schematic read-out circuit under the photoactive layer. The capacitive transimpedance amplifier (CTIA) structure was chosen as the read-out circuit. Moreover, to reduce the output noise, the correlated double sampling (CDS) was implemented in the signal output circuits. CMOS chip fabricated with a 0.18 μm CMOS standard process was realized in the 8x8 pixels. In Figure 3, the uppermost metal (metal 6) of the CMOS standard process was used as the in-plane electrodes and the passivation layer was removed. Before the PVSK film was manufactured on electrodes, atomic layered deposition (ALD)-processed TiO_2 film was deposited on it. The electrodes collected the photocurrent. Photocurrent was read out by the underneath on-chip pixel circuit. The pixel electrodes were interdigital with pixel size 40x40 μm2. The pixel circuits not only amplify the photoelectrical signals, but also provide bias across the pair of electrodes.

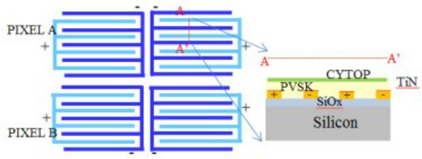

Figure 1. Structure of planar-electrode perovskite photodetector on dummy chip

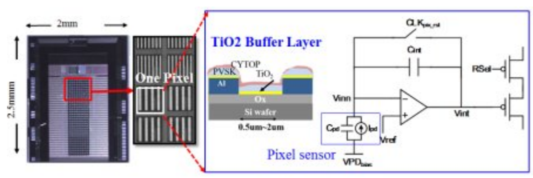

Figure 2. The photo of CIS chip and read-out circuit

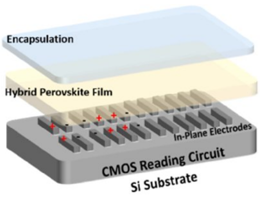

Figure 3. Illustration of perovskite film vertically integrated on the top of signal read-out circuit

Characteristics measurement

The characteristics of the perovskite photodetector pixel on the dummy chip were measured in ambient air and room temperature. Current and voltage (I-V) relationships were measured with a Source Meter Agilent 4156C under the illumination from a microscope 100 W Halogen illuminator. The external quantum efficiency (EQE) over a range of different wavelength was obtained by illuminating periodically modulated monochromatic light on the perovskite photodetector pixel with an optical chopper unit operating at a 85-Hz chopping. The photocurrent signals were extracted with a lock-in technique that used a current preamplifier (Stanford Research Systems) followed by a lock-in amplifier (AMETEK). The EQE measurement was entirely computer controlled, and the monochromatic light intensity was calibrated with an NIST-traceable optical power meter (OphirOptronics).

The specification of the CMOS chip is listed in Table 1. Figure 4 is the illustration of measurement of photoelectric performance for perovskite CMOS chip. The light source was mixed Halogen light and Xe lamp with pan filter.

OPAMP type	N Folded-Cascode
Row time	200 µs
Vref	2.5 V
Gain	80 dB
Power consumption	70 mW
Output data rate	1MHz

Table 1 The specification of the CMOS chip

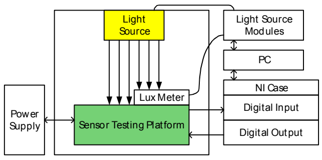

Figure 4. Illustration of measurement of photoelectric performance for perovskite CMOS chip

Results and Discussion

Figure 5 displays the EQE vs. wavelength curve of planar-electrode perovskite photodetector under the biased voltage at 2.5 V. The EQE was more than 1000 % as the irradiation power was in the range of few µW/cm^2. Previously, several planner-electrode structures showing high gain were reported[2,6]. In comparison with the Si-based photodetector, the responsibility of perovskite photodetector covers a wild spectrum range, even between 300-400 nm. This kind of planar-electrode photodetector structure can be modeled as being composed of two Schottky barriers in series[7]. In Figure 6, the asymmetric behavior of I-V curve was observed and the minimum current was not 0 V. It may due to the unequal Schottky barrier which causes by the migration of charged defect ion[8]. It showed excellent on/off ratio of 875 at bias of 2.5V under 0.29 mW/cm^2 irradiation.

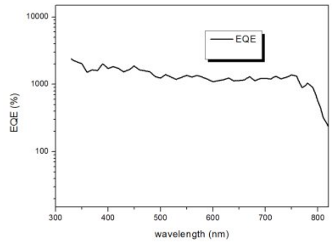

Figure 5. EQE vs. wavelength of the photodetector pixel on the dummy chip

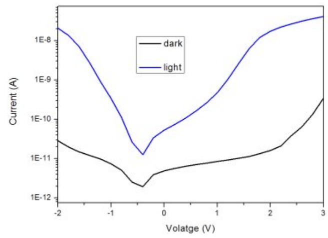

Figure 6. I-V curve of the photodetector pixel on the dummy chip

Figure 7 shows the dark current density vs. voltage of perovskite CMOS image sensor, which was measured by the aid of the on-chip read-out circuit. The dark current density was 2 pA/cm2 at 0.2 V and 10 nA/cm2 at 2 V. The low dark current is helpful to enhance the detectivity. The buffer layer, TiO2 film, effectively reduced the leakage current from the electrode. Figure 8 represents the energy diagram of the planar-electrode perovskite photodetector. Since it is a symmetry structure, we can only choose one material to block either of injection carriers from cathode or anode. TiO_2 increases energy barrier for injection holes from the electrode. It also can enhance the reliability of device to prevent the halogenation of Al electrode. Figure 9 depicts the photodetector pixel performance with different

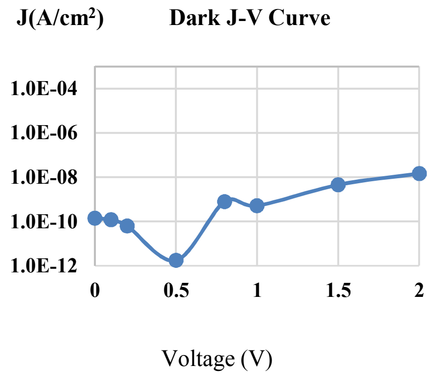

Figure 7. J-V curve in dark

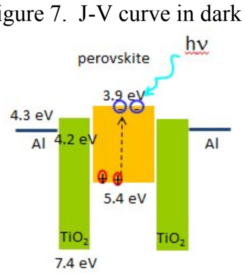

Figure 8. The energy diagram of the planar-electrode perovskite photodetector

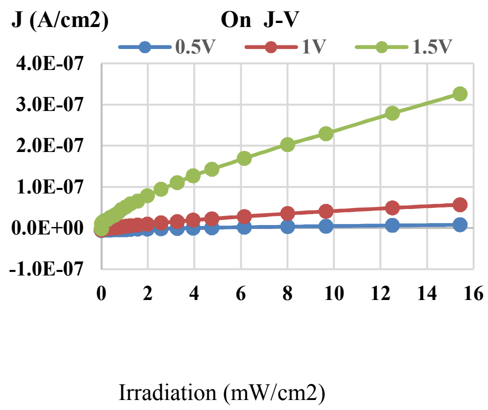

Figure 9 Current density vs. Irradiation curve of perovskite CMOS image sensor

biased voltage under varying irradiation power. It shows that the higher biased voltage lead to the higher optical sensitivity. It means that the gain of this type of photodetector can be adjusted by the biased voltage.

Conclusion

In conclusion, we found that a TiO_2 as a buffer layer in the planar-type electrode perovskite photodetector significantly suppressed the dark current. We have demonstrated the CMOS-compatible peroviskite photodetector with EQE over 1000% and the on/off ratio up to 875 at 2.5V biased voltage under 0.29 mW/cm^2 irradiation. This device structure is designed completely compatible with standard semiconductor process which is easily to integrate with the read-out circuit. These findings demonstrate the possibility of using perovskite active layer for UV enhanced and next generation image sensor technology.

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